AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

On page 3, after paragraph [0011], please add the following new paragraph:

[0012] Fig. 7 is a simplified illustration of a flowchart depicting an embodiment of a method for generating interrupts in a transfer of information between a rake receiver and a processor.

On page 8, after current paragraph [0031], please add the following new paragraphs:

Fig. 7 illustrates an exemplary method for generating interrupts in a transfer of information between a rake receiver and a processor. In step **80**, a rake receiver containing multiple timing fingers de-spreads a received signal. In step **81,** the time rate of the symbol boundaries are determined. In the exemplary embodiment of Fig. 7, if the time rate of symbol boundaries remain constant, data symbols are transferred from the timing fingers to an available data register, as depicted in step **88**. In step **89**, the timing fingers generate interrupts to the processor. Here, the interrupts have a fixed rate and have a rate of generation per unit time independent of a time rate of symbol boundaries. In step **90,** the processor reads data from the available data registers.

If, however, the time rate of symbol boundaries is variable, as depicted in step **81**, the timing fingers write data to an available data register, as shown in step **82**. A counter is incremented by one, as depicted in step **83**. In step **84**, the counter value is checked against a predetermined value. If the counter value equals the predetermined counter value, in step **85**, the counter is decremented based on the predetermined counter value. In step **86**, the timing fingers generate an interrupt resulting from step **85** which may occur at a fixed rate independent of the timing rates of the symbol boundaries. In the exemplary embodiment of Fig. 7, the interrupts are generated asynchronously with respect to the timing rates of the symbol boundaries. In step **87**, the processor may either read more than one first data register and a second data register to which one of the fingers has written or may continue to read one of the first data register and second data register during a given interrupt.

If the a predetermined counter value is not met, as depicted in step **84**, the counter is decremented by one, as depicted in step **91**. In step **92**, the timing fingers generate interrupts. The interrupts are generated at a fixed rate, which are independent and asynchronous with respect to the timing symbol boundaries. In step **93**, the processor reads the data from the available data registers resulting from the interrupts generated in step **92**.